WE CLAIM:

1. A semiconductor device comprising:

an integrated circuit chip having an outline, active and passive surfaces, and active components including a plurality of contact pads, spaced apart by less than 100 μm center to center, on said active surface;

a plurality of electrical coupling members attached to said contact pads, said coupling members selected from a group consisting of gold bumps, copper bumps, copper/nickel/palladium bumps, and z-axis conductive epoxy;

an electrically insulating thin-film interposer having first and second surfaces, a plurality of electrically conductive lines integral with said first surface, a plurality of electrically conductive paths extending through said interposer, contacting said conductive lines and forming exit ports on said second surface;

said chip coupling members attached to said conductive lines, covering an area portion of said first interposer surface; and

encapsulation material protecting said passive chip surface and at least a portion of said first interposer surface not covered by said attached chip.

2. The device according to Claim 1 further having solder balls attached to said exit ports on said second interposer surface.

3. The device according to Claim 1 further having an adhesive non-conductive polymer underfilling any spaces

between said chip coupling members attached to said conductive lines under said chip.

4. The device according to Claim 1 wherein said interposer is a polyimide film.

5. The device according to Claim 1 wherein said interposer has an outline larger than said outline of said chip.

6. The device according to Claim 1 wherein said electrically conductive lines are made of a material selected from a group consisting of copper, copper alloy, or copper plated with tin, tin alloy, silver, or gold.

7. The device according to Claim 1 wherein said coupling member attachment is provided by metal interdiffusion of thermo-compression bonding.

8. The device according to Claim 1 wherein said encapsulation material is a molding compound.

9. The device according to Claim 9 wherein said molding compound has the same outline as said interposer.

10. A semiconductor device comprising:

an integrated circuit chip having an outline, active and passive surfaces, and active components including a plurality of contact pads on said active surface;

a plurality of electrical coupling members attached to said contact pads, said coupling members selected from a group consisting of gold bumps, copper bumps, copper/nickel/palladium bumps, and z-axis conductive epoxy;

an electrically insulating thin-film interposer having first and second surfaces, a plurality of electrically conductive lines integral with said first surface, a plurality of electrically

conductive paths extending through said interposer, contacting said conductive lines and forming exit ports on said second surface;

said chip coupling members attached to said conductive lines, covering an area portion of said first interposer surface; and

encapsulation material protecting said passive chip surface and at least a portion of said first interposer surface not covered by said attached chip.

11. A method of assembling an integrated circuit device, comprising the steps of:

depositing an electrical coupling member of gold, copper, or copper/nickel/palladium on each contact pad of a circuit chip having pads spaced apart by less than 100 μm, center to center;

forming an electrically insulating thin-film interposer by depositing and patterning a plurality of electrically conductive lines on a first surface thereof;

creating a plurality of electrically conductive paths extending through said interposer;

contacting said conductive lines on said first surface and forming exit ports on a second surface of said interposer;

assembling the active surface of said chip onto said first interposer surface such that each of said coupling members is attached to one of said lines, respectively, thereby covering an area portion of said first interposer surface;

encapsulating, with a polymer compound, the passive surface of said chip and at least a portion of

said interposer surface not covered by said attached chip, thereby creating a composite structure having rigidity; and

separating the resulting composite structure into discrete units.

12. The method according to Claim 11 further comprising the step of:

underfilling an adhesive non-conductive polymer into any spaces between said chip coupling members under said chip, which have been formed by said step of assembling said chip onto said interposer, thereby strengthening said assembly.

13. The method according to Claim 11 further comprising the step of:

attaching solder balls to said exit ports on said second interposer surface, after completing said step of encapsulating and before said step of separating.

14. The method according to Claim 11 wherein said step of depositing comprises plating, electro-plating, sputtering, or evaporating.

15. The method according to Claim 11 wherein said step of separating comprises the steps singulating, trimming and forming said composite structure.

16. The method according to Claim 11 wherein said step of assembling comprises the method of thermo-compression gang bonding said chip coupling members onto said interposer lines.